

(B1)

(12) UK Patent Application (19) GB (11) 2 349 505 (13) A

(43) Date of A Publication 01.11.2000

(21) Application No 0007279.3

(22) Date of Filing 24.03.2000

(30) Priority Data

(31) 11084307 (32) 26.03.1999 (33) JP

(71) Applicant(s)

**NEC Corporation**  
(Incorporated in Japan)  
7-1, Shiba 5-Chome, Minato-Ku, Tokyo 108-01, Japan

(72) Inventor(s)

**Mitsunari Sukekawa**

(74) Agent and/or Address for Service

**Mathys & Squire**  
100 Grays Inn Road, LONDON, WC1X 8AL,  
United Kingdom

(51) INT CL<sup>7</sup>

H01L 21/311

(52) UK CL (Edition R)

H1K KHAE KLEXX K1FX K11C1A K3T5 K3T9 K3U6A  
K9N3

(56) Documents Cited

GB 2289984 A EP 0337109 A WO 99/16118 A

(58) Field of Search

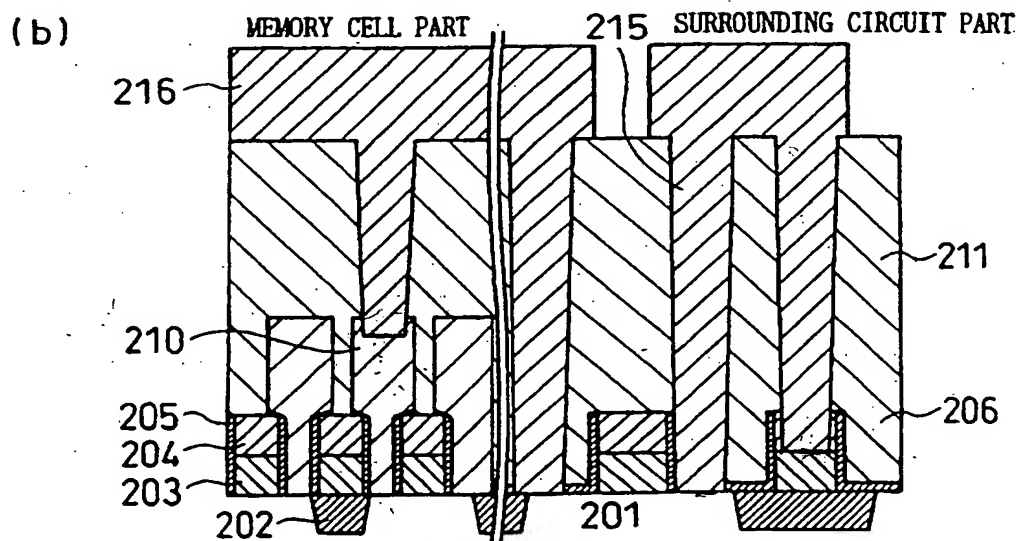
UK CL (Edition R) H1K KDEG KDES KDEX KGFX KHAE  
KLEXX  
INT CL<sup>7</sup> H01L 21/3065 21/3105 21/311 21/60 21/768  
27/108  
ONLINE: WPI, EPODOC, JAPIO

(54) Abstract Title

**Method of fabricating a semiconductor device**

(57) A method for fabricating a semiconductor device, including the steps of: forming a contact hole (208, Figure 2c) so as to cause the etching stopper 205 on the substrate 201 to be exposed; removing an exposed etching stopper 205 on the substrate; filling the contact hole 208 to form a contact plug 210; removing a film [209, Figure 3b] that is deposited on the interlayer insulation film 206, so as to expose the contact plug 210; etching the interlayer insulation film 206 and removing the etching stopper 205 on the gate electrode 203; forming an interlayer insulation film 211; etching the interlayer insulation film 211 so as to expose the etching stopper 205 on a diffusion layer [231, Figure 5a] and etching the insulation film 204 of the gate electrode 203, so as to form contact holes [213, Figure 5a] on the diffusion layer 231 and gate electrode 203; removing the etching stopper 205 exposed on the diffusion layer 231; and, filling the contact hole 213, so as to form the contact plugs 215.

Fig. 6



BEST AVAILABLE COPY

GB 2 349 505 A